

Split-Frame Gimbaled Two-Dimensional MEMS Scanner for Miniature Dual-Axis Confocal Microendoscopes Fabricated by Front-Side Processing

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Abstract—In this paper, we introduce a 2-D microelectromechanical systems scanner for 3.2-mm-diameter dual-axis confocal microendoscopes, fabricated exclusively by front-side processing. Compared to conventional bulk micromachining that incorporates back-side etching, the front-side process is simple and thus enables high device yield. By eliminating the back-side etch window, the process yields compact and robust structures that facilitate handling and packaging. An important component of our front-side fabrication is a low-power deep reactive ion etching (DRIE) process that avoids the heating problems associated with standard DRIE. Reducing the RF etch coil power from 2400 to 1500 W leads to elimination of the spring disconnection problem caused by heat-induced aggressive local etching. In our scanner, the outer frame of the gimbal is split and noncontinuous to allow the scanner to be diced along the very edge of the scanning mirror in order to minimize the chip size (1.8 mm × 1.8 mm). The maximum optical deflection angles in static mode are $\pm 5.5^\circ$ and $\pm 3.8^\circ$ for the outer and inner axes, respectively. In dynamic operation, the optical deflection angles are $\pm 11.8^\circ$ at 1.18 kHz for the outer axis and $\pm 8.8^\circ$ at 2.76 kHz for the inner axis. [2011-0217]

Index Terms—Dual-axis confocal (DAC) microscopy, front-side processing, low-power deep reactive ion etching (DRIE), microendoscope, micromirror, self-alignment, split-frame gimbal, 2-D microelectromechanical systems (MEMS) scanner, vertical combdrive actuator.

I. INTRODUCTION

ADVANCES IN microelectromechanical systems (MEMS) scanner technology have brought enormous impact on development of *in vivo* microscopes. MEMS technology has enabled handheld and endoscopic microscopes that can reach parts of the body not accessible by conventional microscopes. Examples include miniaturized confocal microscopes [1]–[7], optical coherence tomography probes [8]–[10], multiphoton microscopes [11], [12], and photoacoustic imaging probes [13].

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For such miniaturized optical instruments, the MEMS scanners should be small and compact, as well as mechanically robust to facilitate handling and packaging. In addition, it is important to have a simple fabrication process and mass production with high yield to create cost-effective systems.

Several different approaches have been employed for microscope scanners to achieve 2-D scanning with large scan angles. Some of examples are magnetically actuated scanners [7], [9] and electrothermally actuated scanners [10], [13]. Both types of scanners achieve large scan ranges with small driving voltages. However, the integration of a permanent magnet into the magnetically actuated scanners makes its fabrication process serial and often limits the scaling of chip size. The electrothermally actuated scanners have slow scanning speed with resonance frequencies of a few hundred hertz. In addition, its fabrication process requires deposition of several exotic material layers for bimorph beams, and the mechanical rigidity of the beams is restricted by stress in the thin films.

Electrostatic vertical combdrive-actuated scanners [2]–[6], [8], [11], [12], [14]–[16] are widely used due to their high scan speed, low power consumption, and absence of exotic materials. Combdrive-actuated scanners have been fabricated in silicon-on-insulator (SOI) wafers by back-side island isolation [14] or by opening and filling isolation trenches with polysilicon [15]. Two-dimensional scanners made in double-stacked SOI have been also demonstrated to enable electrical isolation and bidirectional tilting on both axes [2]–[6], [11], [16]. In these SOI-based scanners, large mirrors with large scan angles are most often achieved by removing the substrate underneath the scanners to allow larger angular deflections [2]–[6], [8], [11], [12], [14]–[16]. This approach, however, greatly complicates fabrication by increasing the number of masks as well as process steps. In addition, handling and packaging become challenging due to the mechanical fragility introduced by the back-side window.

Previous work reported that back-side etch windows are difficult to replace with cavities fabricated at the start of the process using only front-side processing in double SOI layers [16]. It was observed that double SOI structures suspended over voids in the substrate were stressed to the point of yielding, resulting in broken springs due to lateral etching during deep reactive ion etching (DRIE). However, by controlling the heat generation

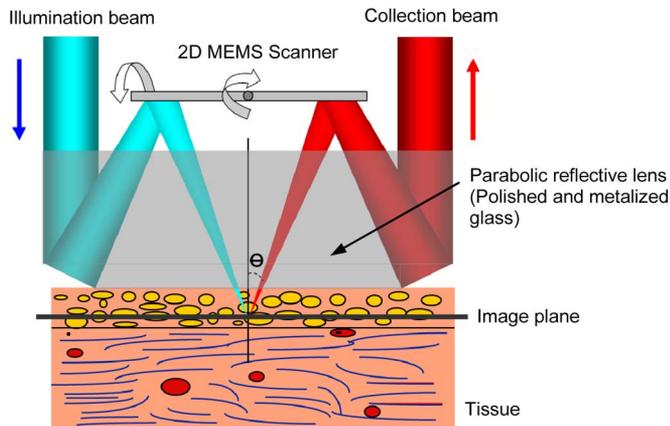


Fig. 1. Schematic of DAC microscope probe.

during etching, we were able to successfully eliminate the spring damage problem in the front-side process.

In this paper, we describe front-side processing that can be applied to fabrication of MEMS scanners and to many other membrane-type structures. The process simplifies the fabrication by eliminating the need of back-side etching, but most importantly, it leads to robust and compact devices that are well suited for miniaturized optical instrumentation. Using this process, we fabricated a combdrive-actuated 2-D MEMS scanner for use in *in vivo* dual-axis confocal (DAC) microscopy, which is an emerging biomedical-imaging technology with high resolution, good tissue penetration, large field of view, and ability to provide both reflectance and fluorescence contrast images [4]. Our scanners allow DAC microscopes to be scaled to 3.2-mm diameter, making them compatible with instrument channels of standard endoscopes.

The organization of this paper is as follows. In Section II, the design of the 2-D MEMS scanner is presented. The details of the front-side processing and thermal analysis of the DRIE process are described in Sections III and IV, respectively. The performance of the fabricated scanner is demonstrated in Section V. Finally, in Section VI, we summarize and conclude our work.

II. SCANNER DESIGN

Front-side processing can be applied to many kinds of micromirrors. Here, we describe a 2-D MEMS scanner for 3.2-mm-diameter DAC microscopes. A schematic of the DAC microscope is shown in Fig. 1. The DAC microscope [2]–[4] achieves large dynamic range and large contrast by separating the illumination and collection beam paths. The low-numerical-aperture parabolic reflective lens provides a long working distance, which allows the MEMS scanner to be placed on the post-objective side for a large field of view. The MEMS scanner not only enables miniaturization of the microscope but also provides real-time 2-D imaging through high-speed point scanning.

Fig. 2 shows our MEMS scanner that consists of a dogbone-shaped micromirror, a split-frame gimbal, and self-aligned electrostatic combdrive actuators. The mirror has two separate reflectors in the same scanning plane for simultaneous scanning

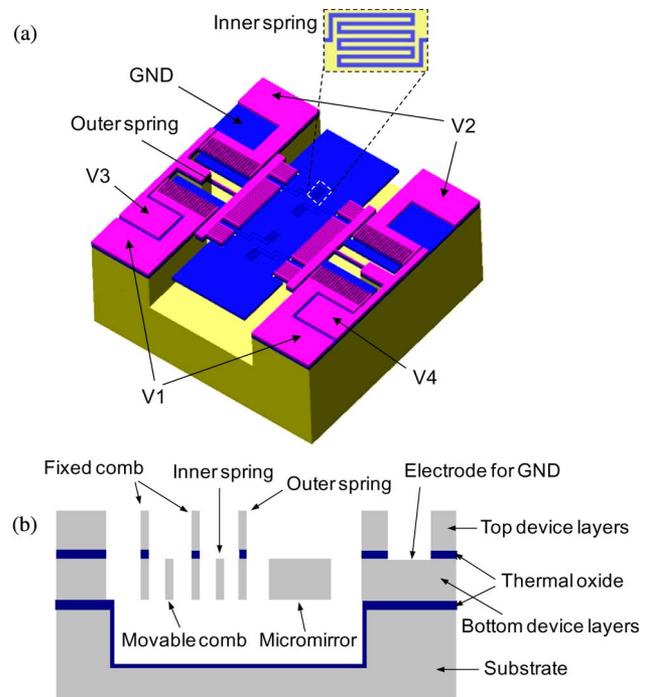


Fig. 2. (a) Schematic of 2-D MEMS scanner. (b) Schematic cross section of the scanner (not to scale).

of the illumination and collection beams. The large and deep cavity created in the substrate allows mirror rotation with large tilt angles. The remaining substrate protects the mirrors and actuators and makes the scanner mechanically robust. The fixed combdrives and outer torsional springs are fabricated in double-stacked SOI, while the micromirror, movable combdrives, and inner torsional springs are made in the bottom device layer. In our dogbone-shaped mirror, the dimensions of the two reflectors are $400\ \mu\text{m} \times 600\ \mu\text{m}$, and the edge-to-edge distance between them is $826\ \mu\text{m}$. The dimensions of the outer springs are $5\ \mu\text{m} \times 250\ \mu\text{m} \times 45.3\ \mu\text{m}$. The inner springs are folded three times, and the dimensions of transverse and longitudinal components are $5\ \mu\text{m} \times 70\ \mu\text{m} \times 25\ \mu\text{m}$ and $5\ \mu\text{m} \times 8\ \mu\text{m} \times 25\ \mu\text{m}$, respectively. For the combdrives, there are 40 movable outer combteeth and 35 movable inner combteeth on each side of the rotation axes with dimensions of $5\ \mu\text{m} \times 130\ \mu\text{m} \times 25\ \mu\text{m}$ in both cases. The comb gaps of the outer and inner combdrives are 5 and $4\ \mu\text{m}$, respectively.

Compared to previously reported micromirrors developed for 5-mm-diameter DAC microscopes [3], our scanner (Fig. 2) has only 33% of the chip area ($1.8\ \text{mm} \times 1.8\ \text{mm}$ for the new design versus $3.4\ \text{mm} \times 2.9\ \text{mm}$ for the previous chip), thus allowing integration into a 3.2-mm-diameter package. The inner springs that previously invaded the reflectors [3] have been moved to the inner connecting area not to obstruct the beam paths. In addition, the inner springs are designed to have a serpentine shape to minimize the torsional stiffness within the small space. The outer frame of the gimbaled 2-D scanner is split to allow the scanner to be diced along the very edge of the mirror for minimization of the chip size. A conventional gimbal frame wrapping around the mirror would inevitably increase the chip size by a few hundred micrometers. The structural stability of

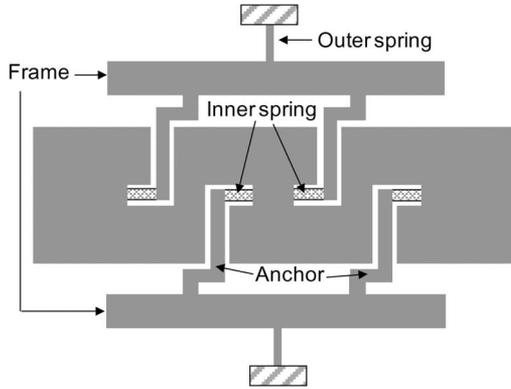


Fig. 3. Simplified schematic of the split-frame gimbal (top view).

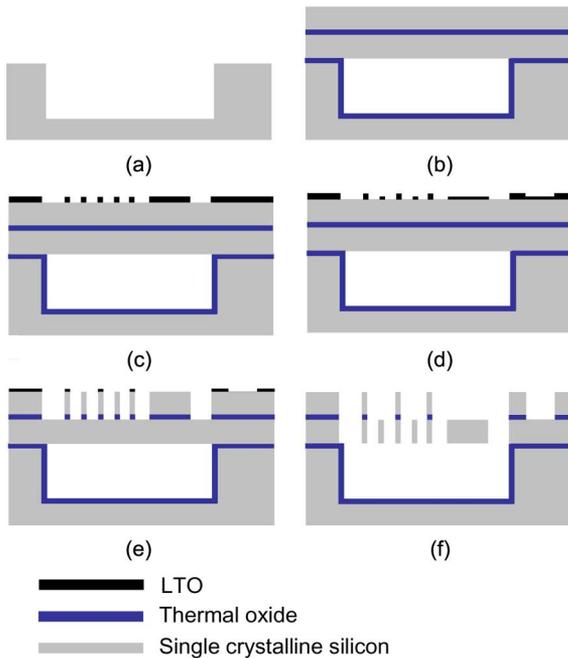


Fig. 4. Process flow of 2-D MEMS scanner. (a) DRIE to create a large cavity (mask 1). (b) Thermal oxidation, fusion bonding, grinding, and polishing. (c) Self-alignment mask patterning of LTO (mask 2). (d) Partial etch of LTO hard mask (mask 3). (e) DRIE of the top device layer and plasma oxide etching. (f) DRIE of the bottom device layer defined by mask 2, followed by plasma oxide etching.

the split-frame gimbal is maintained by connecting the two halves of the split frame using four anchors and the inner springs via the mirror. Fig. 3 shows a simplified schematic of the gimbal design. For clarity, the serpentine inner springs are replaced with straight beams in this figure.

III. FABRICATION

Our scanner is fabricated exclusively by front-side processing, as shown in Fig. 4. The following sections describe each fabrication step in detail.

A. Creating a Large Cavity

The process starts with creating a large cavity in a Si wafer. A 6000-Å-thick oxide layer is grown on the wafer by wet

oxidation at 1000 °C and patterned as a hard mask. Then, a 280- μm -deep trench is created by DRIE. Such deep large-area (1780 μm \times 860 μm) etches often lead to grass formation [17]. Grassing can be eliminated by applying high bias power with no electromagnet bias, which leads to enhanced ion bombardment at the base of the trench.

B. Wafer Fusion Bonding, Grinding, and Polishing

There are three main parameters that must be controlled for successful direct wafer bonding—the curvature, the waviness, and the surface roughness of the wafers [18]. Reducing the curvature of the wafers minimizes the necessary surface bonding energy to overcome the strain energy present in the wafers before bonding. In order to reduce the surface energy required for a successful bonding, ultraflat wafers with very low total thickness variations ($TTV < 2 \mu\text{m}$) are used.

Low surface roughness is extremely important for a successful wafer bonding. In preparation for wafer bonding, the oxide hard mask is removed by buffered oxide etching (BOE) with careful etching time control. Excessive overetching is detrimental because the BOE can roughen the bonding surface, resulting in poor bond quality [19]. A 0.31- μm -thick new oxide layer is then grown on the cavity wafer with wet oxidation at 1100 °C. This thermal oxide layer serves as an etch stop layer, an insulation layer, and a bonding enhancer.

Before bonding, both the cavity wafer and the SOI wafer are chemically activated by immersing the wafers in an ammonium hydroxide solution at around 70 °C [20], in order to make the bonding surfaces hydrophilic. The wafers are then bonded under vacuum in a wafer bonder (Model SB6 from SUSS MicroTec AG, Germany) at a temperature of 50 °C and a force of 600 N applied to the 4-in wafers. The bonded wafers are inspected by an IR camera to check that no voids are present. Finally, the bonded wafers are annealed at a temperature of 1050 °C to increase the bond strength. After this, the bonded SOI wafer is ground and polished with an accuracy of $\pm 2 \mu\text{m}$ to create the two device layers. The resulted thicknesses of the upper device layer, the buried oxide (BOX), and the lower device layer are 20, 0.31, and 25 μm , respectively.

C. Control of LTO Thickness for Self-Alignment Etching

For self-alignment of the comb fingers and springs, a single low-temperature oxide (LTO) is deposited at 400 °C and patterned with two masks sequentially [16]. The first mask (mask 2) removes the full thickness of the LTO, while the second (mask 3) removes only a fraction of the LTO, so that the remaining thin oxide layer can be utilized to define the structures in the bottom device layer.

In our design, 0.85- μm -thick LTO was deposited on the top surface, and some part of LTO was partially etched to 0.24 μm through the double-masking process. These LTO thicknesses were carefully determined by considering the thicknesses of each device layer as well as the etch selectivity between oxide and silicon, so that the original LTO and the partially etched LTO can create device structures in both device layers and only in the bottom device layer, respectively. For successful pattern

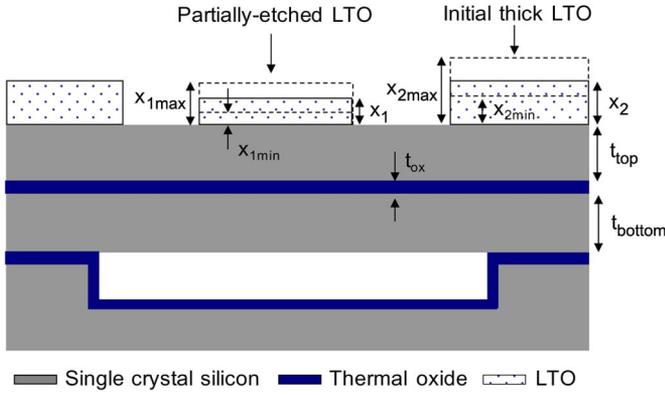


Fig. 5. Allowable LTO thicknesses for self-alignment etching.

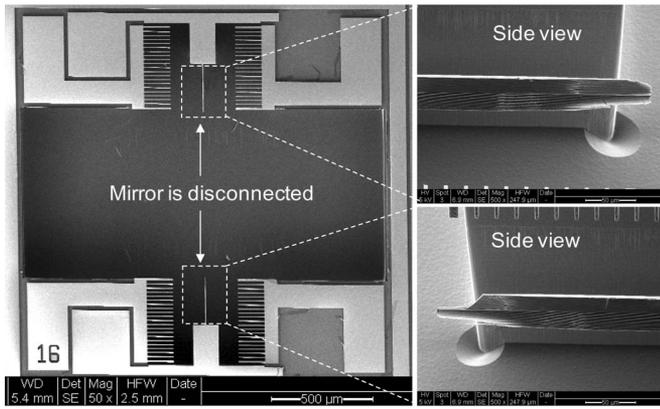


Fig. 6. SEM images of damages caused during the release DRIE step.

transfer and self-alignment, the thicknesses of LTO should be in the following ranges (Fig. 5):

partially etched LTO

$$1.2 \frac{t_{top}}{n} \leq x_1 \leq \frac{t_{top}}{n} + t_{ox} \quad (1)$$

original LTO

$$\begin{aligned} 1.2 \frac{t_{top}}{n} + 1.2 t_{ox} + 1.2 \frac{t_{bottom}}{n} &\leq x_2 \\ &\leq 1.2 \frac{t_{top}}{n} + 2.2 t_{ox} + \frac{t_{bottom}}{n} \end{aligned} \quad (2)$$

where $t_{ox} >$ buffer LTO for 20% overetching of Si. In our DRIE, the selectivity of oxide to silicon (n) was about 250. Therefore, the required LTO thicknesses should be as follows: $0.096 \mu\text{m} < x_1 < 0.406 \mu\text{m}$ and $0.588 \mu\text{m} < x_2 < 0.878 \mu\text{m}$. Our design settings satisfy these conditions.

D. Self-Alignment DRIE and Wafer Heating Control

Using the LTO as a hard mask, sequential etching of the top device layer, BOX, and the bottom device layer is conducted to pattern the device structures. The fabrication is completed with mirror release after this self-alignment DRIE step.

A key point in front-side processing is controlling the wafer heating during DRIE. Fig. 6 shows the damage caused in the release DRIE step [Fig. 4(f)] when the DRIE setting in column 1

TABLE I
DRIE RECIPES

	Overheating	Successful process
SF6/O2 Flow	450sccm/45sccm	450sccm/45sccm
C4F8 Flow	100sccm	100sccm
Etch/Passivation cycle time	3sec/2sec	3sec/2sec
Pressure (etch/passivation)	34mTorr/12mTorr	34mTorr/12mTorr
RF Coil power (etch/passivation)	2400W/1000W	1500W/1000W
Bias power (etch/passivation)	45W/0W	45W/0W

of Table I was used. It is found that the distal end of the beam springs is consumed aggressively and resulted in pop-up of the micromirror during etching.

The main cause of the aggressive local etching is heating in the suspended structure [21]. Large amount of heat is generated during plasma etching due to ion bombardment and exothermic chemical reaction. The substrate has a large heat capacitance, so heating does not become problematic in the bulk area. In the suspended mirror, however, the heat leads to abrupt temperature increases, due to the high thermal resistance of the springs. The high temperature not only reduces the deposition rate of the sidewall inhibitor but also increases the etch rate according to Arrhenius relation [22]. It leads to catastrophic damage to slender structures that are close to or connected to the suspended structure, as shown in our fabrication. Section IV gives a detailed discussion of the heating effect in DRIE.

Our strategy for solving this problem was to lower the DRIE process temperature by decreasing the RF coil power, which determines the plasma density. Fig. 7 shows the wafer temperature dependence on RF coil power. The temperature of the wafer surface was measured by using temperature labels (Omegalabel Temperature Labels) attached on the wafer. By reducing the etch coil power of 2400 W in step (e) in Fig. 4 to 1500 W in the release etching step (f), the etch rate for 4- μm -gap trench in bulk silicon decreased from 6 to 4.5 $\mu\text{m}/\text{min}$, and the wafer temperature was lowered by 16 $^\circ\text{C}$. This leads to much larger temperature decrease in the suspended mirror due to low heat capacitance of the mirror and high thermal resistance of the outer springs. As a consequence, the fabrication could be successfully completed, as shown in Fig. 8. For patterning the top device layer [Fig. 4(e)], low-power etching is not necessary because the bottom device layer provides a large heat conduction path.

E. Dicing

Dicing the chips is another critical step. The device chip size is designed to be 1.8 mm \times 1.8 mm for packaging in a 3.2-mm-diameter housing, and the margin between the edges of the mirror to the dicing lines is only $\sim 80 \mu\text{m}$. In contrast to MEMS scanners with back-side etch windows, front-side processed mirrors preserve the substrate and can be diced through the cavity at the very edges of the mirrors, therefore keeping the chip size at a minimum, as shown in Fig. 9. This compact chip size cannot be achieved with a back-side etch window

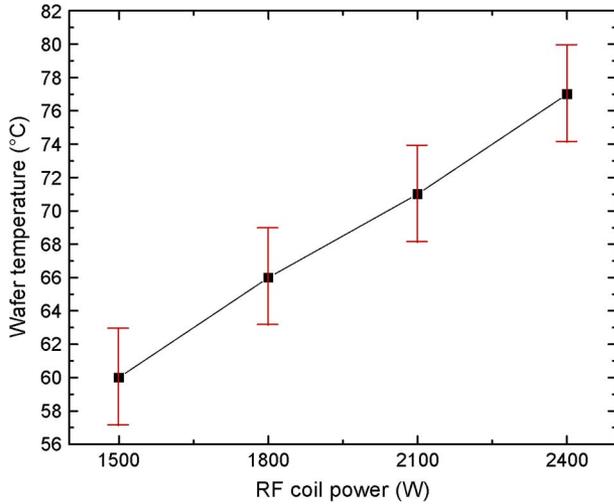


Fig. 7. Wafer temperature versus RF etch coil power.

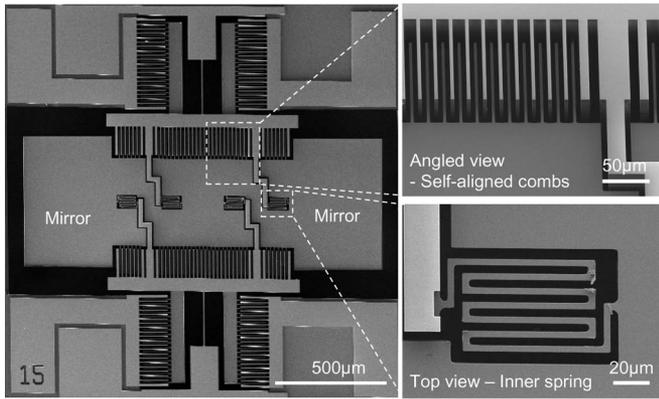


Fig. 8. SEM image of the fabricated 2-D MEMS scanner.

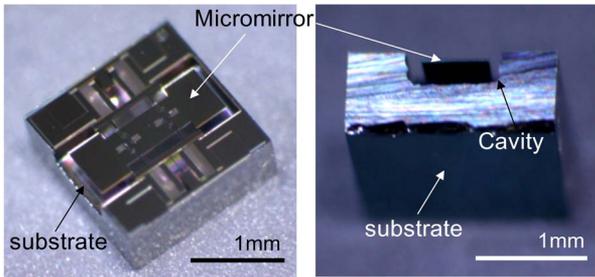


Fig. 9. Microscope image of the fabricated mirror.

because the substrate will be separated into two pieces if dicing through the cavity. The solid substrate of the diced chip (Fig. 9) prevents damage to the mirror when the chip is bonded to the housing, provides better thermal properties, and allows a variety of bonding technologies to be used. Furthermore, the mirror damping is not affected by chip bonding, leading to improved repeatability.

F. Metallization of the Mirror

High light efficiency is desired to increase the signal strength [23]. To improve the reflectivity, the mirror is metallized with aluminum. Aluminum does not require an adhesive layer for

coating on silicon surface, thus minimizing the stress generated by thin-film deposition. A 15-nm-thick aluminum layer is deposited on top of the mirror by blanket evaporation. At 633-nm wavelength, the reflectivity of the bare Si mirror (30%) increases to 83% when the mirror is coated with a 15-nm aluminum layer. Since the light reflects off the mirror twice in DAC microscopy, this enhances the light collection efficiency by a factor of 7.65.

IV. THERMAL ANALYSIS OF DRIE PROCESS

In DRIE, temperature rise leads to degraded sidewall passivation as well as enhanced etch rates according to Arrhenius equation [22], thus resulting in deteriorated etching profiles. Therefore, it is important to investigate the temperature differences in the suspended structures, in order to understand the variations in local etching during DRIE.

We conducted a thermal analysis of our scanner structure by considering the thermal effects of both ion bombardment and exothermic reaction. In an inductively coupled plasma (ICP) system, the heat generated from the ion bombardment per unit area is given by [21]

$$Q_i = n_i q V_{\text{bias}} \sqrt{\frac{q T_e}{m}} \quad (3)$$

where n_i , q , V_{bias} , T_e , and m are the ion density, the electric charge, the sheath bias voltage, the electron temperature, and the mass of reactive ions (SF_3^+), respectively. The parameter values relevant to ICP DRIE are given in [21]. The heat generated by the exothermic reaction can be expressed as

$$Q_e = r c_{\text{Si}} \Delta H_{\text{SiF}_4} \quad (4)$$

where r is the etch rate in Arrhenius equation [22], c_{Si} is the concentration of Si ($\sim 8.3 \times 10^4 \text{ mol} \cdot \text{m}^{-3}$), and ΔH_{SiF_4} (1358 kJ/mol) is the heat generated by chemical reaction between Si and the fluorine radicals. Only part of exothermic heat is transferred onto the etching surface because the rest is taken by volatile SiF_4 molecules. In our analysis, 50% of the exothermic heat was assumed to be absorbed onto the surface.

Based on these sources of heat generations, the temperature distribution in the scanner can be calculated using the energy conservation equation

$$\rho c_p \frac{\partial T}{\partial t} = k \nabla^2 T \quad (5)$$

where ρ , c_p , k , and t are the silicon wafer density ($2.3 \text{ g} \cdot \text{cm}^{-3}$), specific heat of silicon ($703 \text{ J} \cdot \text{kg}^{-1} \cdot \text{K}^{-1}$), thermal conductivity of silicon ($149 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$), and time, respectively. COMSOL Multiphysics was used for simulation of the heat dissipation during DRIE at RF etch coil powers of 2400 W (overheating case) and 1500 W (successful case). The temperature of the entire structure before the mirror release is set to be 77 °C according to our measurement in Fig. 7. In order to establish the point in time when problematic heating starts in the overheating case, we simulate two different scenarios: 1) the case that 2- μm -thick layers are left in the bottom device layer between comb fingers and between serpentine inner spring

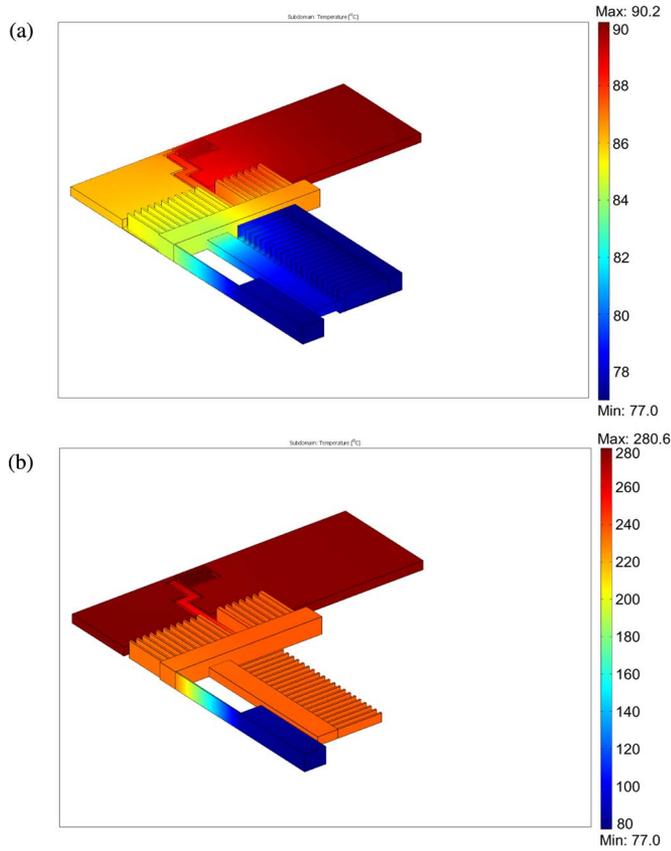


Fig. 10. Simulation of temperature gradient during DRIE with an etch coil power of 2400 W. (a) Two-dimensional scanner model with $2\text{-}\mu\text{m}$ -thick layers remaining between comb fingers and between serpentine spring beams (incomplete release case). (b) Two-dimensional scanner model with complete release of the scanner structure except the serpentine inner spring area due to local etch rate variation by ARDE.

beams while all other sparse pattern areas (e.g., around outer springs and around the mirror) are etched through due to aspect-ratio-dependent etching (ARDE) and 2) the case with complete release of the scanner structure except the serpentine inner spring area (incomplete etch-through was assumed around the inner springs, considering local etch rate variation by ARDE). In the first case [Fig. 10(a)], the maximum temperature difference between the substrate and the suspended mirror is only $13.2\text{ }^{\circ}\text{C}$, indicating that no serious variation in local etch rate will occur. The heat generated during DRIE is effectively dissipated throughout both the outer springs and the remaining thin layer between comb fingers, which are still connected to the substrate.

The second case represents a worst case situation with the largest etch speed variations. In this model, the outer springs are the only heat conduction paths to the substrate, working as a bottleneck for heat dissipation. Therefore, the temperatures of the mirror and the outer springs in the mirror side become very high, reaching $280.7\text{ }^{\circ}\text{C}$ and $230.6\text{ }^{\circ}\text{C}$, respectively [Fig. 10(b)]. This large temperature increase makes the etch rate 3.5–4.6 times faster than the rate before the structure release. For the mirror and the outer spring in the mirror side, the temperature variations over time are simulated and plotted in Fig. 11. Both temperatures reach the steady state in less than 1 s. This abrupt temperature change causes very aggressive consumption of

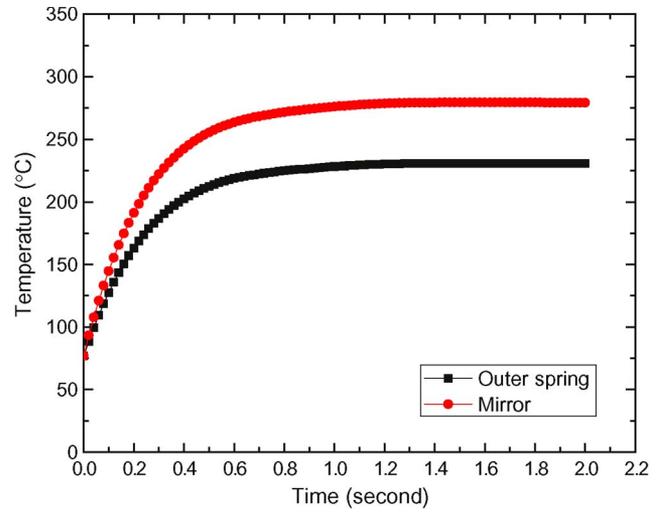


Fig. 11. Temperature of released scanner structure versus time during DRIE with an etch coil power of 2400 W.

Si structures during the 3-s etch cycle (Table I) before the passivation cycle starts. Our simulation results (Figs. 10 and 11) prove that the heating problem begins during overetching after the complete release of the suspended structure.

In the overetching situation [Fig. 10(b)], the most serious damages occur around the inner springs where the highest temperatures are induced in the suspended mirror. However, in our fabrication, the effect of the increased etch rate in these parts is not significant due to the high aspect ratio of the inner spring patterns. The outer springs are broken first, even before complete etch-through of the inner springs. The aggressively etched hot spots of the outer springs are vulnerable to high shear and thermal stress induced by high temperature gradients. When the stress exceeds the mechanical tolerance, the outer springs are broken.

Intermittent cooling of the wafer during DRIE cannot provide an effective cooling solution, because of the rapid increase of temperature in the suspended mirror. To overcome the heating problem, we used a lowered RF etch coil power (1500 W) during DRIE to decrease the process temperature. The appropriate RF coil power to achieve high fabrication yield was found experimentally. According to our simulation, the temperatures of the mirror and the outer springs in the mirror side are lowered to $178\text{ }^{\circ}\text{C}$ and $150\text{ }^{\circ}\text{C}$, respectively, when the low-power DRIE is used for a scanner model shown in Fig. 10(b). The reduced temperature decreases the etch rate by 40%–46% compared to the etch rate with 2400-W coil power. In our fabrication, this low-power DRIE led to fabrication yield of around 91% by preventing disruption of the outer springs.

V. DEVICE CHARACTERIZATION

The use of single-crystal-silicon surfaces for the mirrors increases reflectivity and minimizes scattering loss. The curvature and the surface roughness of this mirror are measured by a WYKO optical surface profiler (NT1100, Veeco). Our measurement [24] shows that the mirror has a radius of curvature of 1.9 m with peak-to-valley surface deformation less than $0.1\text{ }\mu\text{m}$.

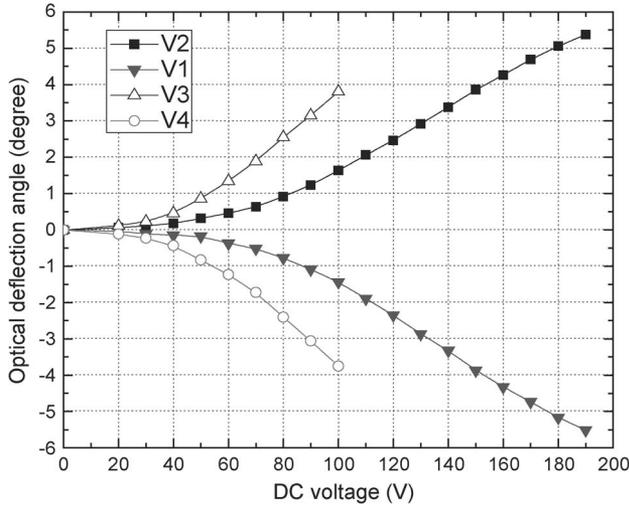


Fig. 12. Static optical deflection curves. $V1$ and $V2$ are for the outer axis, and $V3$ and $V4$ are for the inner axis.

The surface roughness is 5.3 nm, ensuring high optical quality. This result shows that our mirror has better optical quality than the previously reported mirror (the surface roughness = 25 nm, and the radius of curvature = 60 cm), which is designed for 5-mm-diameter DAC microscopes [3].

Fig. 12 shows the optical deflection angle measured in static mode. The optical deflection angles range from -5.5° at $V1 = 190$ V to 5.4° at $V2 = 190$ V for the outer axis and from -3.8° at $V4 = 100$ V to 3.8° at $V3 = 100$ V for the inner axis. The maximum deflection angles of the torsional scanner are limited by pull-in of combdrives [25]. In our design, the outer springs are stiffer against in-plane twist (dominant pull-in mechanism) than the inner springs. In addition, the outer comb gap is wider than the inner comb gap. Therefore, the outer torsional motion is more resistant to pull-in, resulting in larger tilt angles.

The dynamic response of the scanner (Fig. 13) was characterized by applying driving voltages of $(62 + 37 \sin 2\pi ft)$ V and $(68 + 37 \sin 2\pi ft)$ V for the outer and inner axes, respectively. A position sensitive detector was used to measure the optical deflection of the reflected beam. The optical deflection angles at resonance were $\pm 11.8^\circ$ at 1.18 kHz for the outer axis and $\pm 8.8^\circ$ at 2.76 kHz for the inner axis. In addition to the fundamental torsional resonance frequency of f_0 , subharmonic modes at $f_0/3$ and $f_0/2$ and the second harmonic at $2f_0$ are observed for both axes. For the outer axis, mode coupling was observed at $f_0/3$ (350 Hz), while relatively large rotational modes were obtained at $f_0/2$ (550 Hz) and $2f_0$ (2.23 kHz) as obtained at the fundamental resonance. Similar responses were observed for the inner axis, but the rotational modes at $f_0/2$ (1250 Hz) and $2f_0$ (5 kHz) were not large. The subharmonic and second harmonic modes are likely caused by the nonlinear relationship between voltage and electrostatic force of combdrive actuators [26].

To verify the reliability of the scanner, we tested repeatability and stability by operating it in dc and ac modes, respectively. In dc, the optical deflection curves in Fig. 12 could be consistently obtained while repeating the static voltage sweep over 50 times. The scanner was operated at resonances to test its stability over

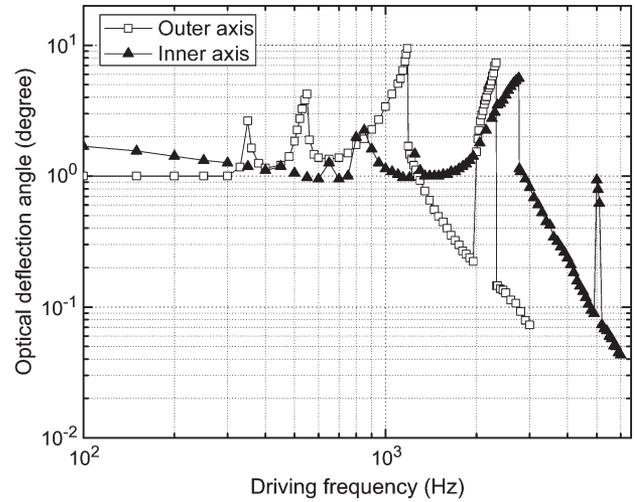


Fig. 13. Dynamic frequency response of MEMS scanner.

time. We found no measurable fluctuations in the total optical deflection angles for about 100 h, proving high stability of our scanner.

For safety in endoscopic use, our scanners on miniature circuit boards will be encapsulated in the DAC probe and will be sealed with medical-grade UV-curing glue. The electrostatic MEMS scanner itself draws minimal current (in nanoamperes) and will be well insulated as demonstrated in our 10- and 5-mm-diameter microscopes [4]. As an added safety measure, we will implement an overload protection circuit that shuts down the system if the current exceeds the safety threshold.

VI. CONCLUSION

We have developed front-side processing for fabrication of 2-D MEMS scanners by minimizing the wafer heating during the release DRIE step. Front-side processing greatly simplifies the fabrication and reduces cost. In addition, by preserving the integrity of the substrate, this process achieves compact and robust designs and significantly facilitates handling and packaging of the chips for miniaturized optical instrumentation. Using this new process, we successfully fabricated a split-frame gimballed 2-D MEMS scanner for 3.2-mm-diameter DAC microendoscopes. Its compact design and small chip size ($1.8 \text{ mm} \times 1.8 \text{ mm}$), enabled by front-side processing, will provide high-resolution 2-D imaging in a miniaturized microendoscope.

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